Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A controller for a memory having at least one memory cell, that involves a higher cost for writing than for reading, said memory cell being allocated a first address information and adapted to store memory data, said memory controller comprising:

a register connected with said memory, and comprising register space for write data and for address information allocated thereto;

a write controller connected with said register and said memory, and adapted to:

receive a write request comprising said first address information and first write data allocated thereto;

ascertain whether said first address information is stored in said register;

if yes, compare said first write data with second write data of an earlier write request in said register allocated to said first address information;

if no, compare said first write data with said memory data allocated to the first address information;

forward said first address information and said first write data to said register, respectively;

initiate a write operation of said first or second write data, respectively, from said register to said memory, if the first or second write data, respectively, is different from said memory data.

2. (previously presented) The memory controller of claim 1, wherein said register is a FIFO register.

3. (currently amended) The memory controller of claim 1, further comprising a read controller connected with said register and said memory, and adapted to receive a read request comprising said first address information ascertain whether said first address information is stored in said register forward said read request to said register or said memory, depending on whether or not, respectively, said first address information is stored in said ~~register,~~ register.

4. (previously presented) The memory controller of claim 3, wherein said write controller is adapted to send to said read controller a read request upon reception of said write request, said read request comprising said first address information contained in said write request.

5. (previously presented) The memory controller of claim 1, wherein the write controller is adapted to allocate a flag indicative of the result of the comparison to said first write data and to transfer the flag to said register along with said first write data and said first address information, and to initiate a write operation to the memory only for first write data for which the flag is indicative of a difference between said first write data and said memory data or said second write data, respectively.

6. (previously presented) The memory controller of claim 5, wherein the write controller is adapted to ascertain whether said register is full or empty.

7. (previously presented) The memory controller of claim 6, wherein the write controller is adapted to initiate at least one write operation from the register to the memory after assessing that the register is full.

8. (previously presented) The memory controller claim 1, wherein the write controller is adapted to initiate a write operation from the register to the memory after assessing that the register is not empty and in case there is no pending write request.

9. (previously presented) The memory controller of claim 1, wherein the write controller is adapted to perform the comparison of said first write data with said second write data or said memory for at least one bit at a time.

10. (previously presented) The memory controller of claim 9, wherein the write controller is adapted to perform the comparison byte by byte or bit by bit.

11. (previously presented) The memory controller of claim 9, wherein the write controller is adapted to perform the comparison bit by bit.

12. (previously presented) The memory controller of claim 9, comprising an XOR-Gate with a first input for said first write data and a second input for said memory data or said second write data, respectively, and an output port connected with the write controller.

13. (previously presented) The memory controller of claim 9, wherein the write controller is adapted to forward said first address information and said first write data to said register after receiving at least one logical "TRUE"-signal from the output of the XOR-Gate.

14. (previously presented) A memory device comprising a memory with at least one non-volatile memory cell and a memory controller according to claim 1.

15. (previously presented) A memory device according to claim 1, wherein said memory comprises memory cells from the group of MRAM and FERAM.

16. (canceled)

17. (previously presented) A method for writing to a non-volatile memory using a writing queue, said memory comprising at least one memory cell for storing memory data, said memory cell being uniquely allocated at least a first memory address and requiring a higher cost for writing than for reading, comprising the steps of:

receiving a write request comprising the first address information and first write data allocated thereto;

ascertaining whether said first address information is stored in said writing queue;

if yes, comparing said first write data with second write data in said writing queue allocated to said first address information;

if no, comparing said first write data with said memory data allocated to the first address information;

forwarding said first address information and said first write data to said writing queue if the first write data is different from the second write data or said memory data, respectively; and

writing said first write data from said writing queue to said memory cell corresponding to said first address.

18. (previously presented) The method of claim 17, wherein said first write data of different write requests is written from said writing queue to said memory according to a First-in-First-Out rule.

19. (previously presented) The method of claim 17, further comprising the steps

receiving a read request comprising said first address information ascertaining whether said first address information is stored in said writing queue;

forwarding said read request to said writing queue or said memory, depending on whether or not, respectively, said first address information is stored in said writing queue;

receiving from said writing queue or said memory, respectively, said writing queue data or said memory data allocated to said first address information.

20. (previously presented) The method of claim 17, comprising a step of performing a read request upon reception of said write request, said read request comprising said first address information contained in said write request.

21. (previously presented) The method of claim 17, comprising a step of ascertaining whether said writing queue is full and/or whether said writing queue is empty.

22. (previously presented) The method of claim 21, comprising a step of writing from the writing queue to the memory after assessing that the register is full.

23. (previously presented) The method of claim 21, comprising a step of writing from the writing queue to the memory after assessing that the writing queue is not empty and in case there is no pending write request.

24. (previously presented) The method of claim 17, comprising a step of comparing at least one bit at a time of said first write data and of said second write data or said memory data.

25. (previously presented) The method of claim 24, wherein said comparing step comprises a step of performing an XOR-operation between said first write data and said memory data or said second write data, respectively.

26. (canceled)